IN THE CLAIMS

Please amend the claims as follows.

1. (Currently Amended) An electrostatic discharge (ESD) protection circuit, suitable for use on the I/O pad, the ESD protection circuit comprising:

a silicon controlled rectifier (SCR) circuit, which comprises a first connection terminal, a second connection terminal, and a third connection terminal, wherein the first connection terminal and the second connection terminal are respectively connected to the I/O pad and a ground voltage, so as to discharge the electrostatic charges; and

an anti-latch-up circuit, which comprises a fourth connection terminal, a fifth connection terminal, and a sixth connection terminal, respectively coupled to a voltage source, the ground voltage, and the third connection terminal of the SCR circuit, wherein the sixth connection terminal of the anti-latch-up circuit is directly connected to the third connection terminal of the SCR circuit, wherein a voltage rising rate at a node of the anti-latch-up circuit determines whether or not to trigger the SCR circuit and thereby prevent ~~is whereby an anti-latch-up signal is sent from the sixth connection terminal to the SCR circuit for preventing~~ latching up of the SCR circuit during normal operation~~, wherein SCR circuit is triggered by an ESD event, and wherein the I/O pad is not directly connected to the voltage source and the anti-latch-up circuit~~.

2. (Original) The ESD protection circuit of claim 1, further comprising:

a first diode, having a first input end and a second input end, respectively connected to the ground voltage and the I/O pad; and

a second diode, having a first input end and a second input end, respectively connected to the I/O pad and a voltage source.

3. (Previously Presented) The ESD protection circuit of claim 1, wherein the SCR circuit comprises:

a P-type substrate;

an N well, formed in the p-type substrate;

a first P+ doped region, formed in the P-type substrate and coupled to the ground voltage;

a first N+ doped region, formed in the P-type substrate, adjacent to the first P+ doped region, and coupled to the ground voltage;

a second N+ doped region, formed between the P-type substrate and the N well, adjacent to the first N+ doped region, coupled via the third connection terminal of SCR circuit to the sixth connection terminal of the anti-latch-up circuit, serving as a guard ring to collect electrons to avoid latch up when the anti-latch-up circuit sends the anti-latch-up signal through the sixth connection terminal to the third connection terminal of the SCR circuit during normal operation, and floating when the anti-latch-up circuit sends no signal to the SCR circuit during an ESD event;

a second P+ doped region, formed in the N well, adjacent to the second N+ doped region, and coupled to the I/O pad; and

a third N+ doped region, formed in the N well, adjacent to the second P+ doped region, and coupled to the voltage source;

wherein a diode is coupled to the second P+ doped region and the I/O pad at one end and coupled to the other end.

4. (Original) The ESD protection circuit of claim 3, wherein the anti-latch-up circuit comprises:

a capacitor, having a first contact end and a second contact end, respectively coupled to the second N+ doped region and the ground voltage; and

a resistor, having a first end and a second end, respectively coupled to the voltage source and the second N+ doped region.

Claims 5-12 (Canceled).

13. (Previously Presented) The ESD protection circuit of claim 1, wherein the anti-latch-up signal sent from the sixth connection terminal to the SCR circuit comprises a voltage signal.

Claim 14 (Canceled).

15. (New) The ESD protection circuit of claim 1, wherein a RC delay time of the anti-latch-up circuit is smaller than a voltage rising time of an IC power but greater than a voltage rising time of an ESD pulse.